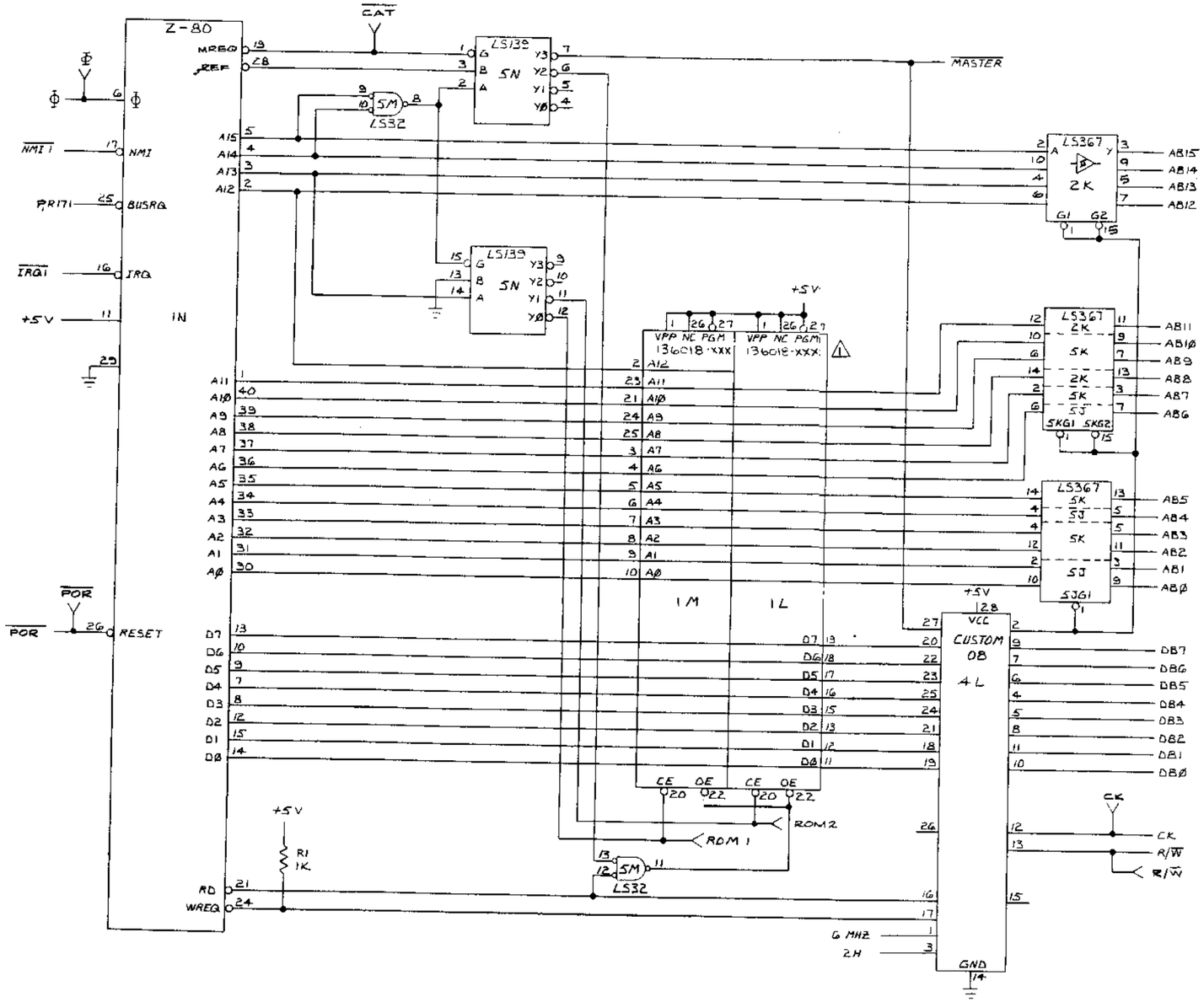
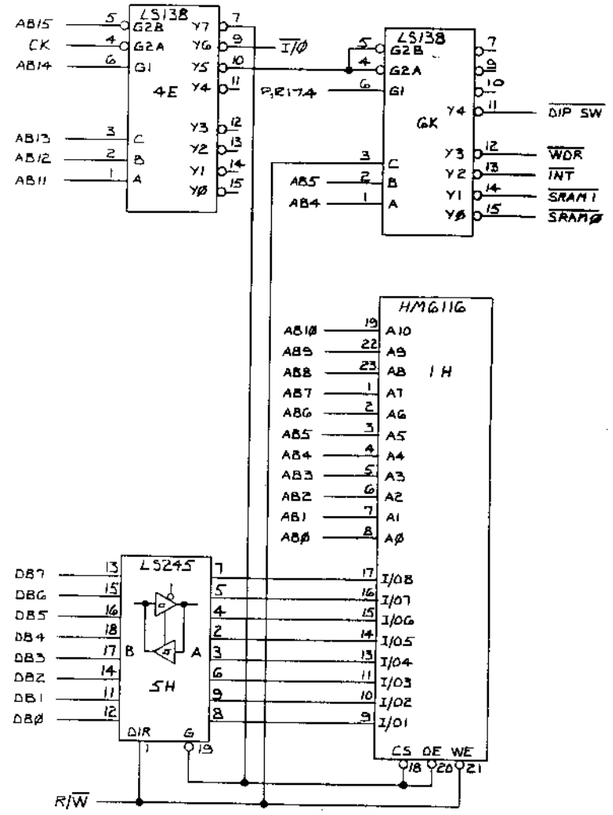
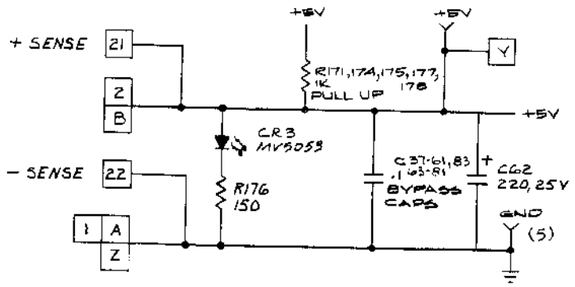
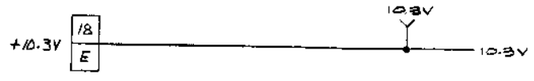
MEMORY MAP

HEXA-DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES																R/W	DATA BUS SIGNAL LINES								FUNCTION
	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	
CPU PCB																										
0000–1FFF	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	MASTER PROGRAM
0000–2FFF	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	MASTER PROGRAM
0000–1FFF	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	MOTION PROGRAM
0000–1FFF	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	SOUND PROGRAM
6800	0	1	1	0	1					0	0	0		0	0	0	W									SOUND RAM 0
6810	0	1	1	0	1					0	0	1		0	0	0	W									SOUND RAM 1
6820	0	1	1	0	1					0	1	0		0	0	0	W									CLEAR
6821	0	1	1	0	1					0	1	0		0	0	1	W									CLEAR
6822	0	1	1	0	1					0	1	0		0	1	0	W									$\overline{\text{NMION}}$
6823	0	1	1	0	1					0	1	0		0	1	1	W									$\overline{\text{RESET}}$
6824–6827	0	1	1	0	1					0	1	0		A	A	A	W									NOT USED
6830	0	1	1	0	1						1	1					W									$\overline{\text{WDR}}$
6840	0	1	1	0	1						A	A		A	A	A	R							D	D	$\overline{\text{DIP SW}}$
7000	0	1	1	1	0												R/W	D	D	D	D	D	D	D	D	$\overline{\text{I/O}}$ DECODE
7100	0	1	1	1	0												R/W									$\overline{\text{I/O}}$ CONTROL
7800	0	1	1	1	1	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM}}$
VIDEO PCB																										
8000–8FFF	1	0	0	0		A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM 2S}}$
9000–9FFF	1	0	0	1		A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM 2R}}$
A000–AFFF	1	0	1	0		A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM 2P}}$
B000–BFFF	1	0	1	1		A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM 1}}$
C000–CFFF	1	1	0	0		A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	$\overline{\text{RAM 2}}$
D000	1	1	0	1													R									$\overline{\text{PAL}}$
F000	1	1	1	1												0	R/W									$\overline{\text{BB0}}$ (Read) $\overline{\text{BS0}}$ (Write)
F001	1	1	1	1												1	R/W									$\overline{\text{BB1}}$ (Read) $\overline{\text{BS1}}$ (Write)



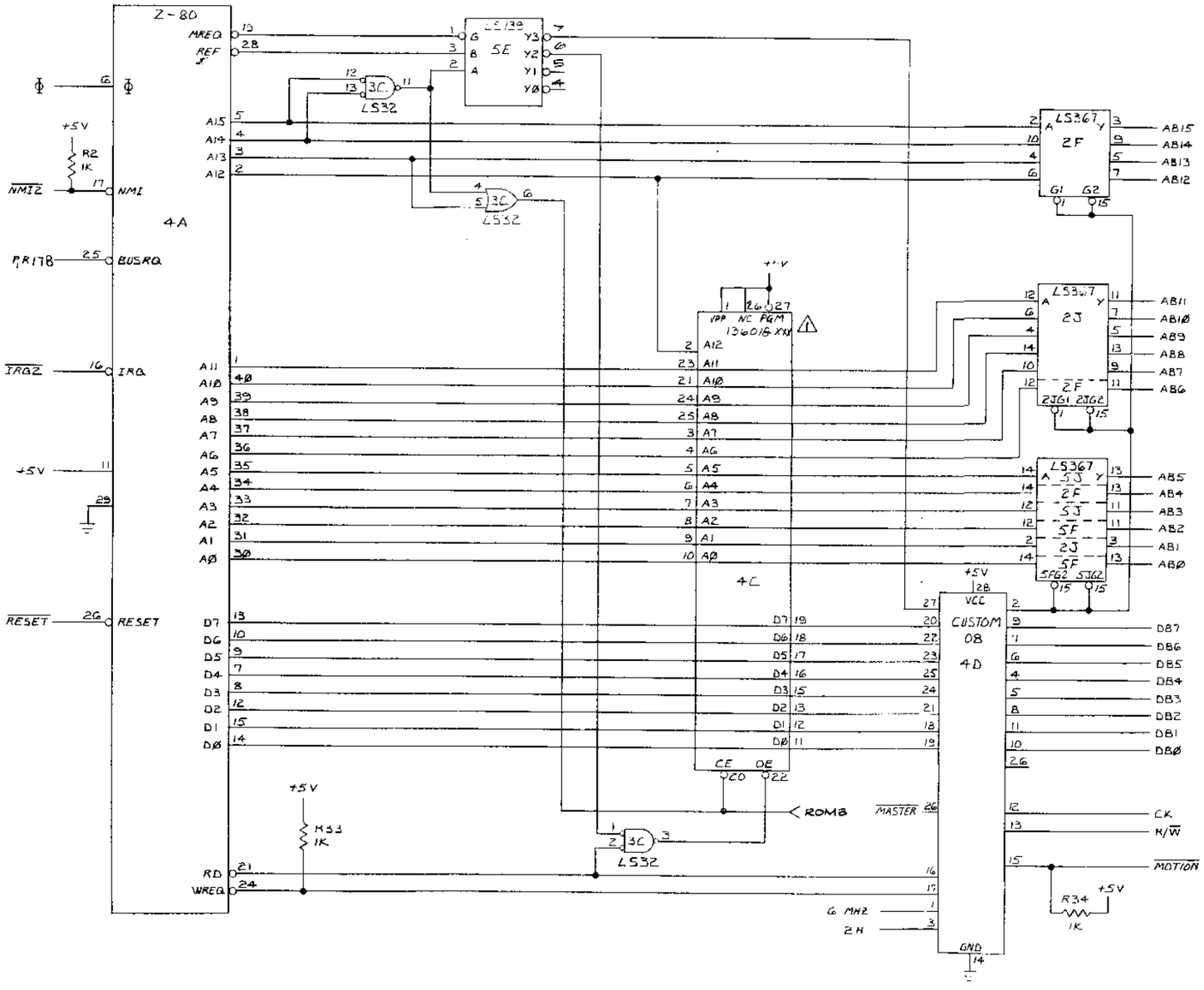


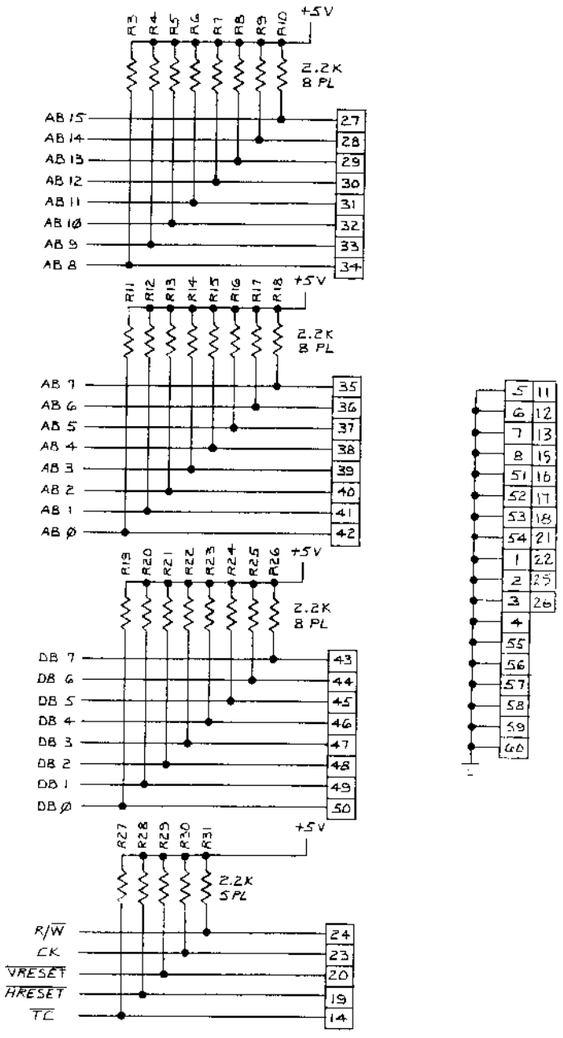




Xevious CPU PCB Schematic Diagram

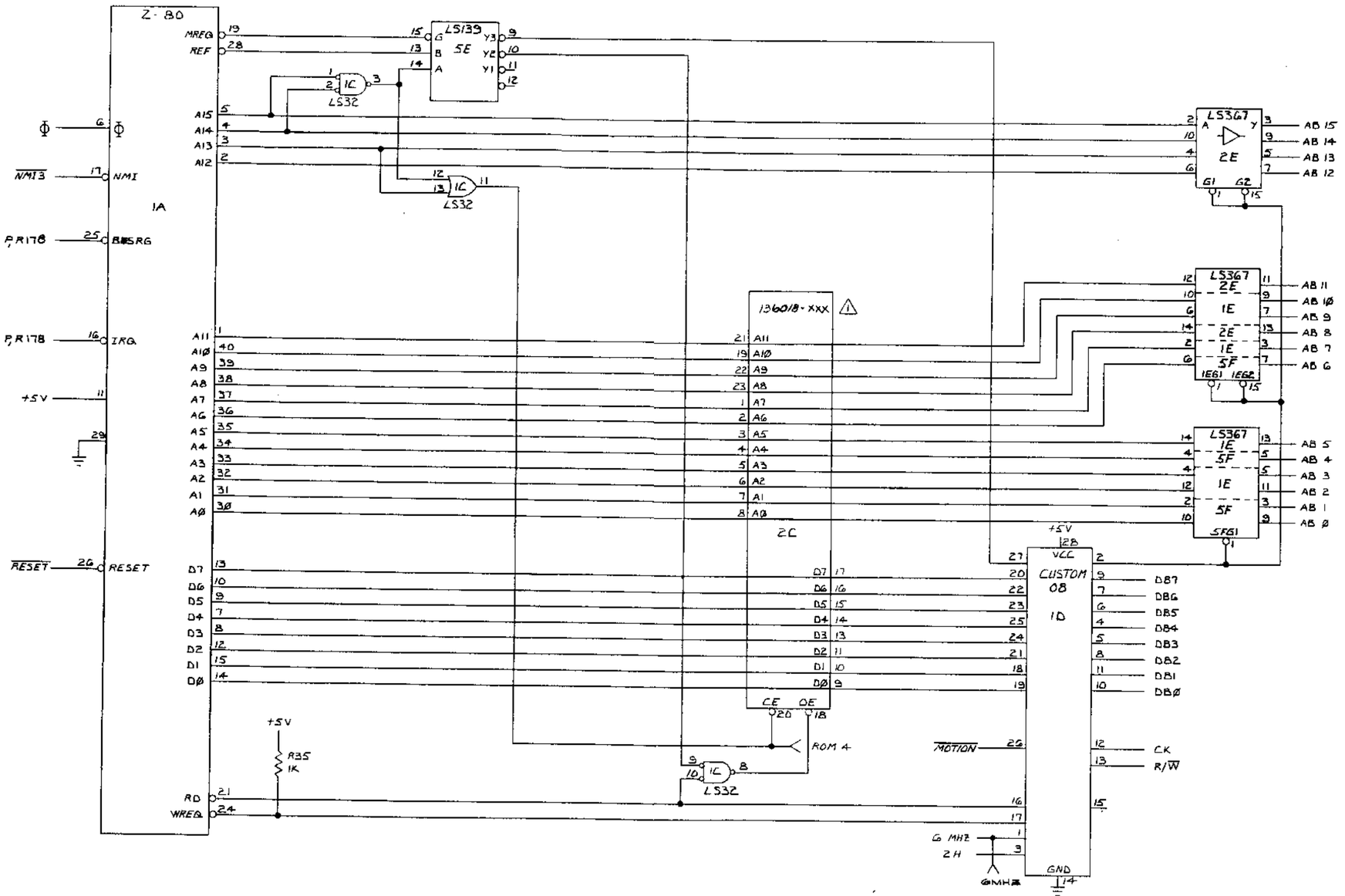
Sheet 4A





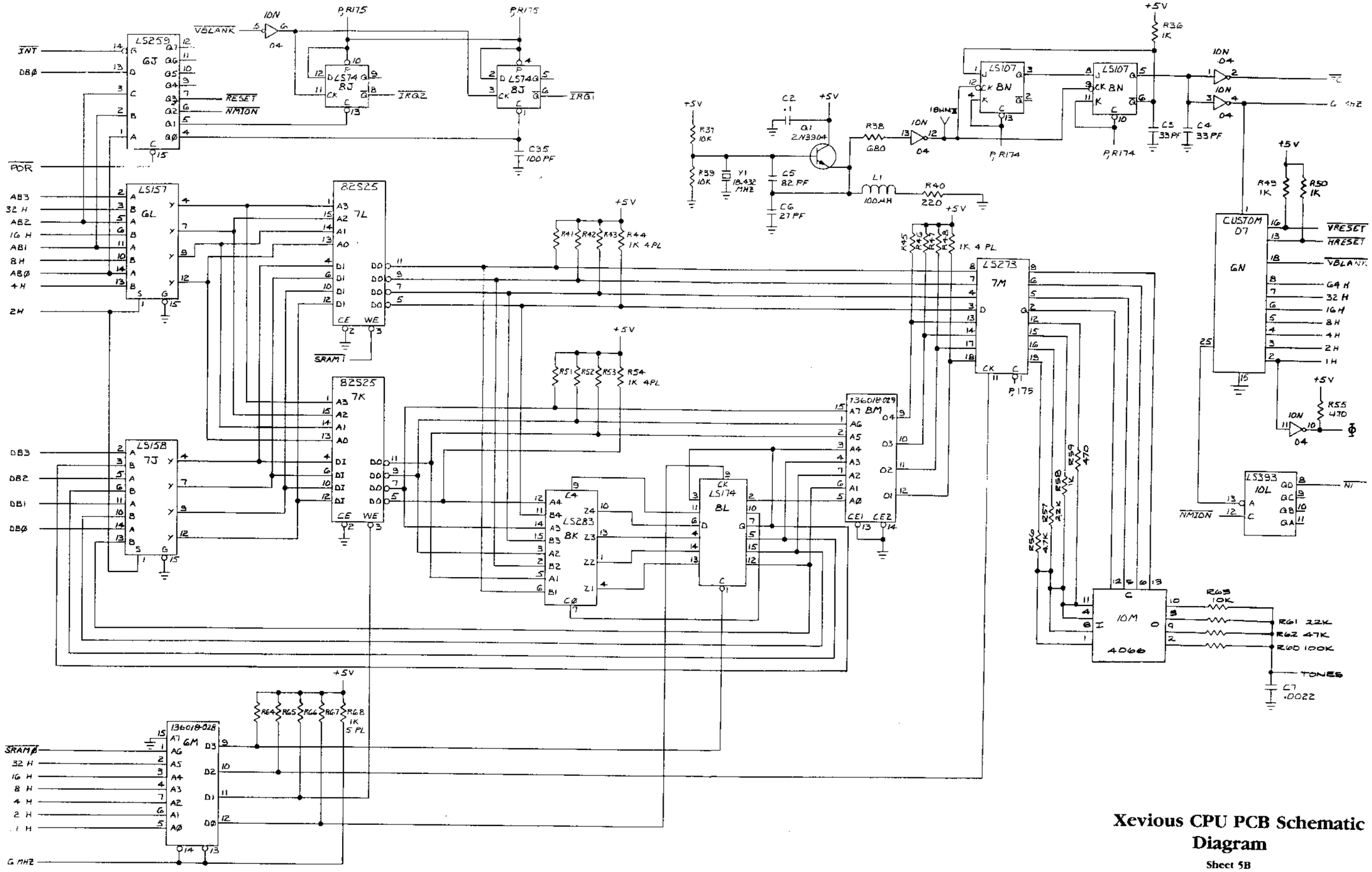
Xevious CPU PCB Schematic Diagram

Sheet 4B



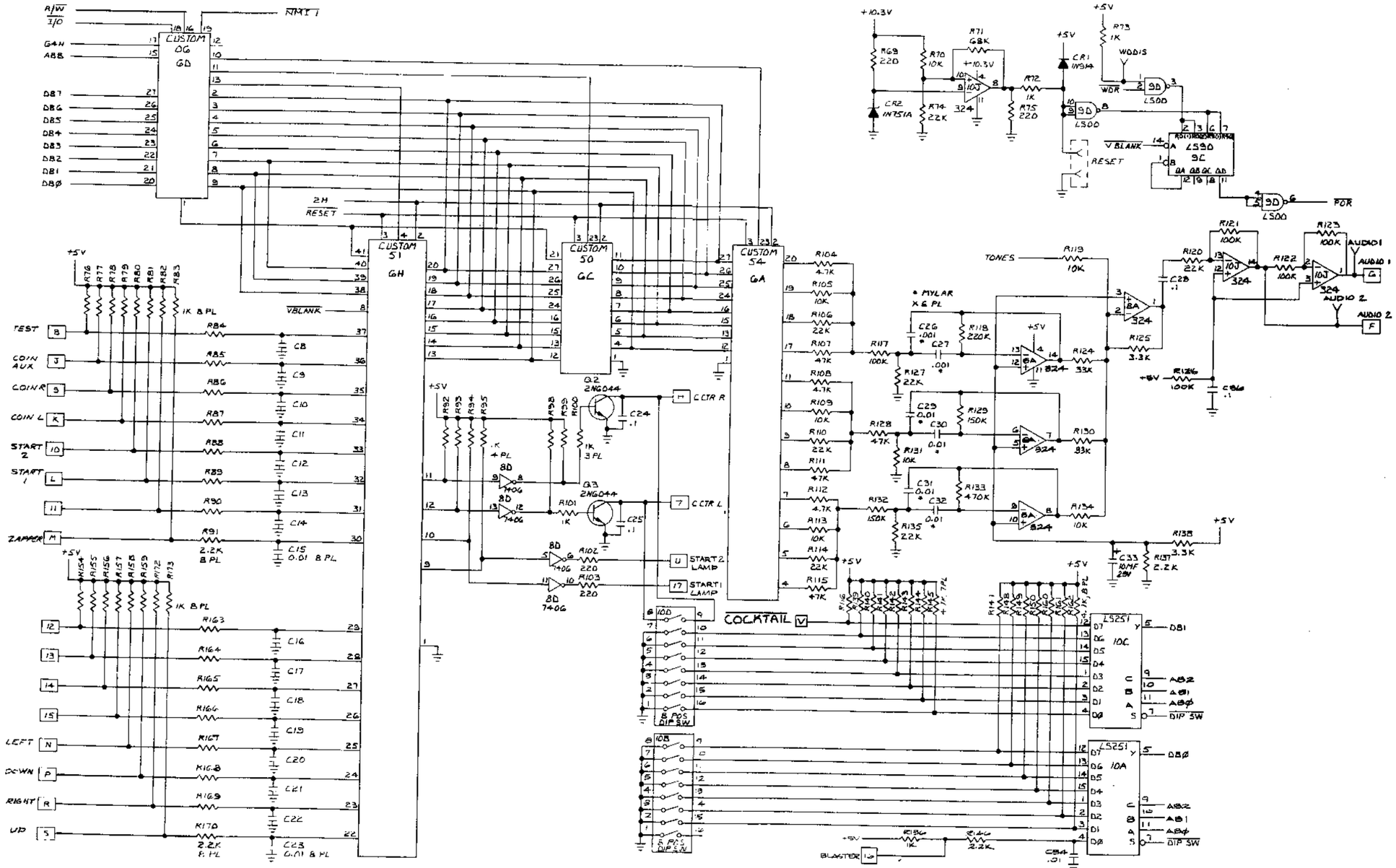
Xevious CPU PCB Schematic Diagram

Sheet 5A



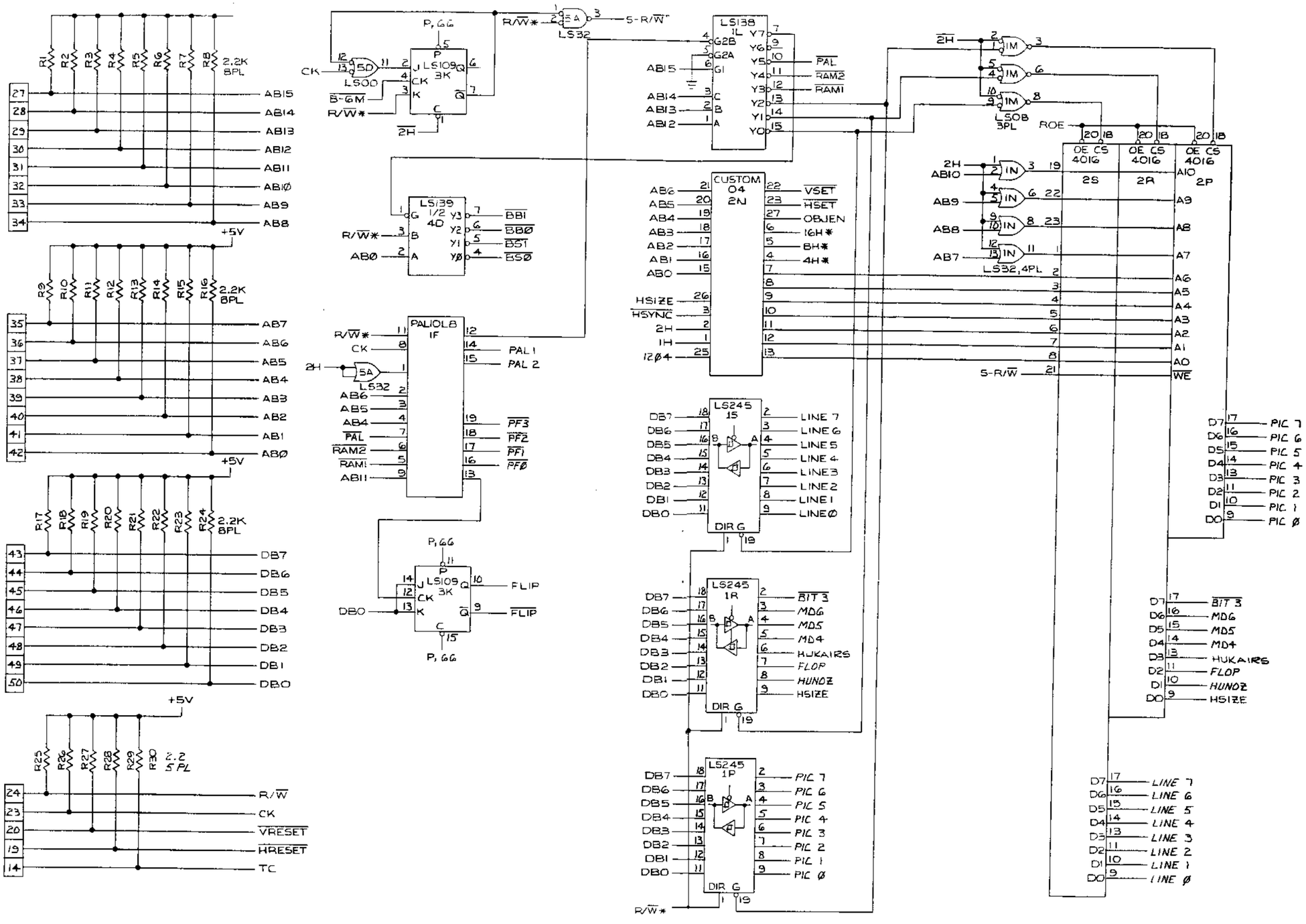
Xevious CPU PCB Schematic Diagram

Sheet 5B



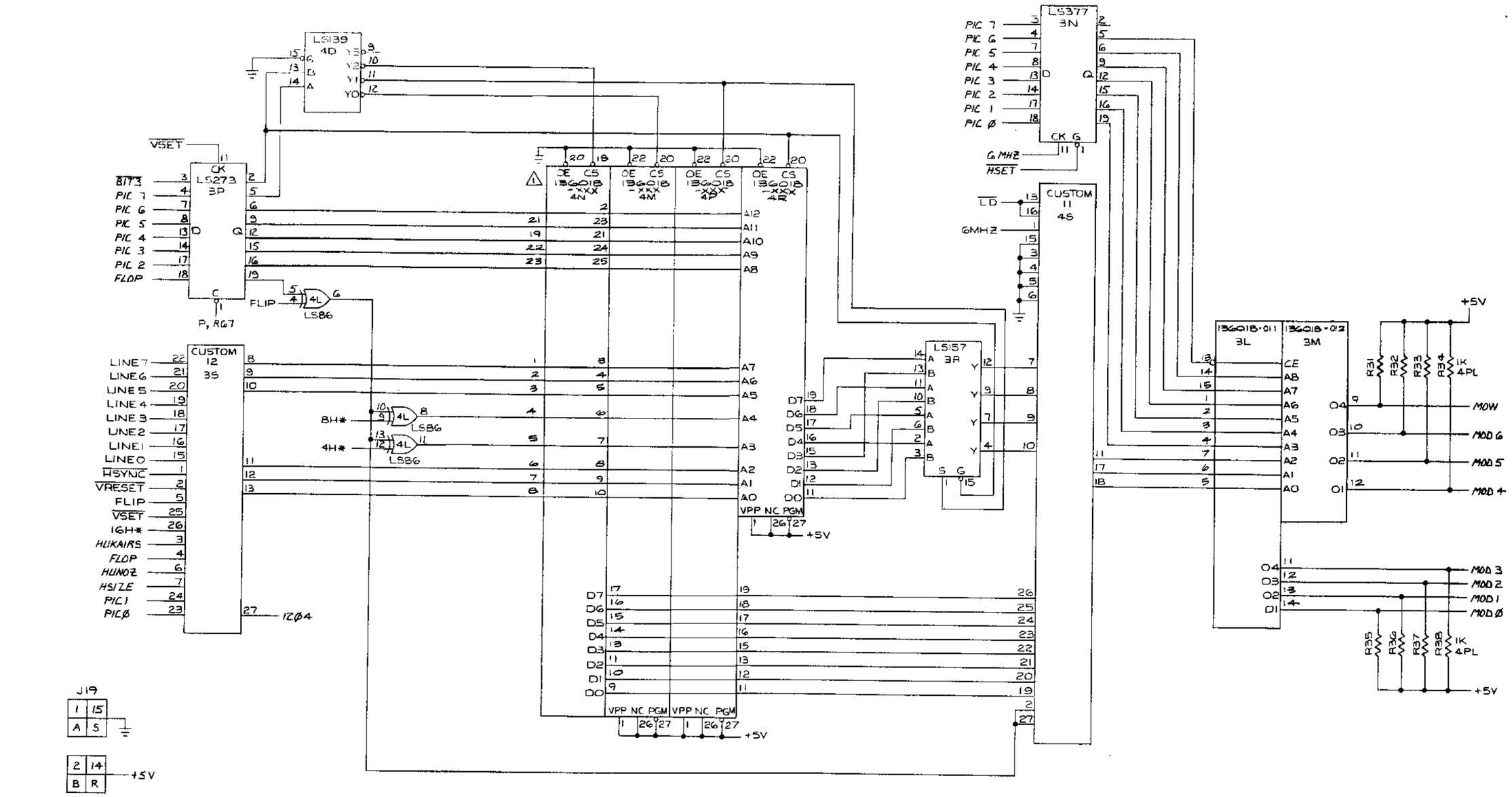
Xevious CPU PCB Schematic Diagram

Sheet 6A



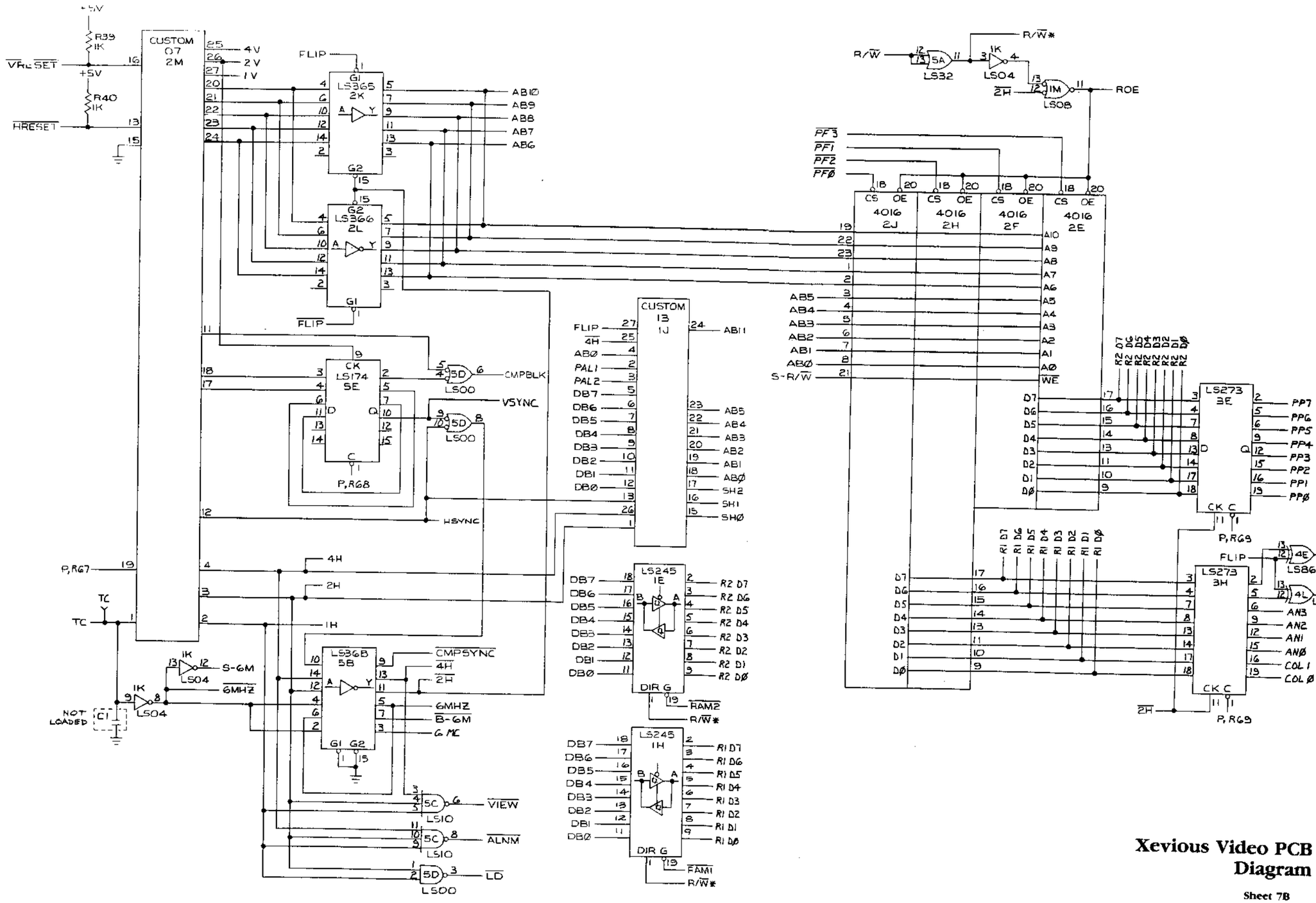
Xevious Video PCB Schematic Diagram

Sheet 6B



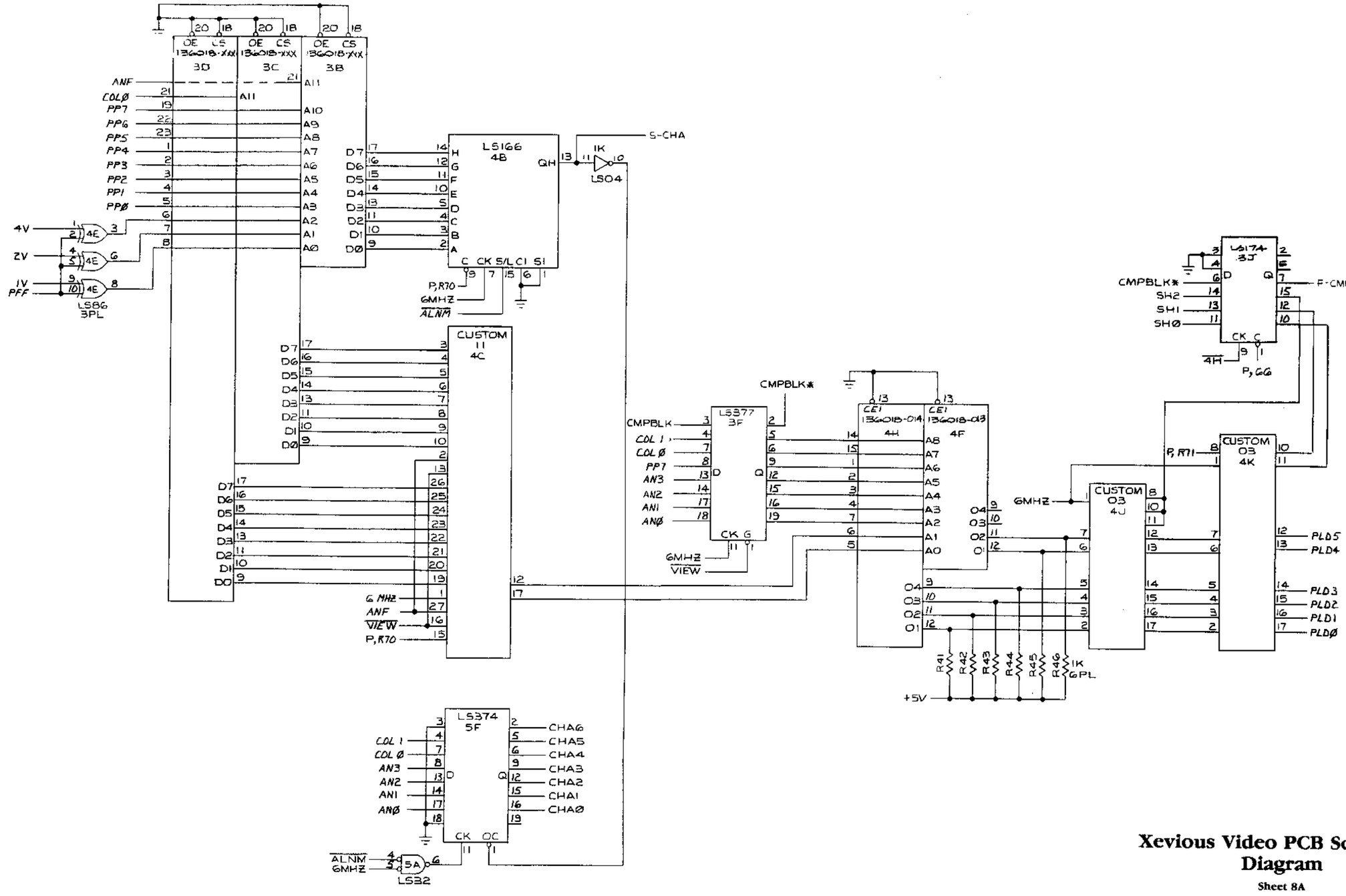
Xevious Video PCB Schematic Diagram

Sheet 7A



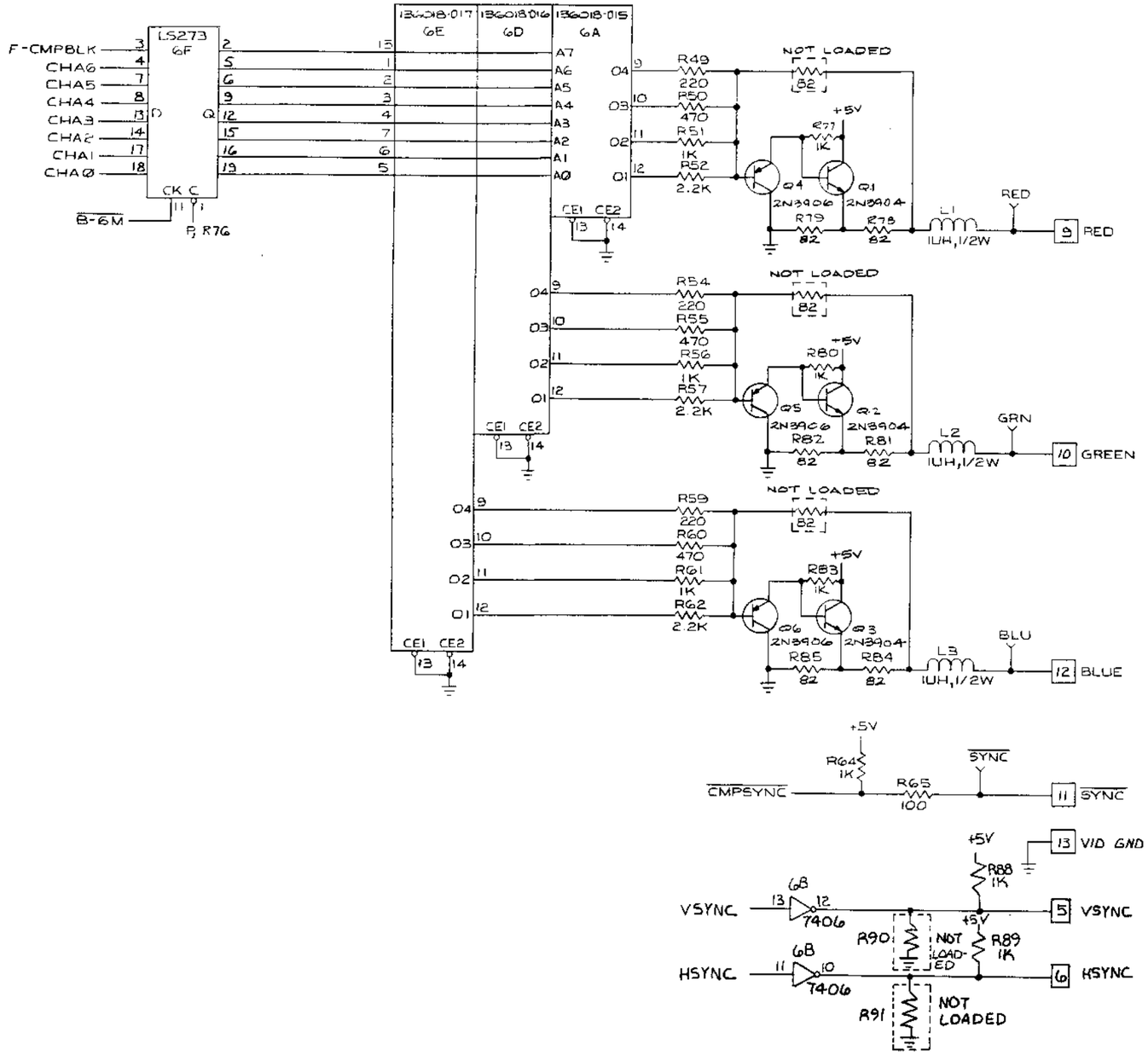
Xevious Video PCB Schematic Diagram

Sheet 7B



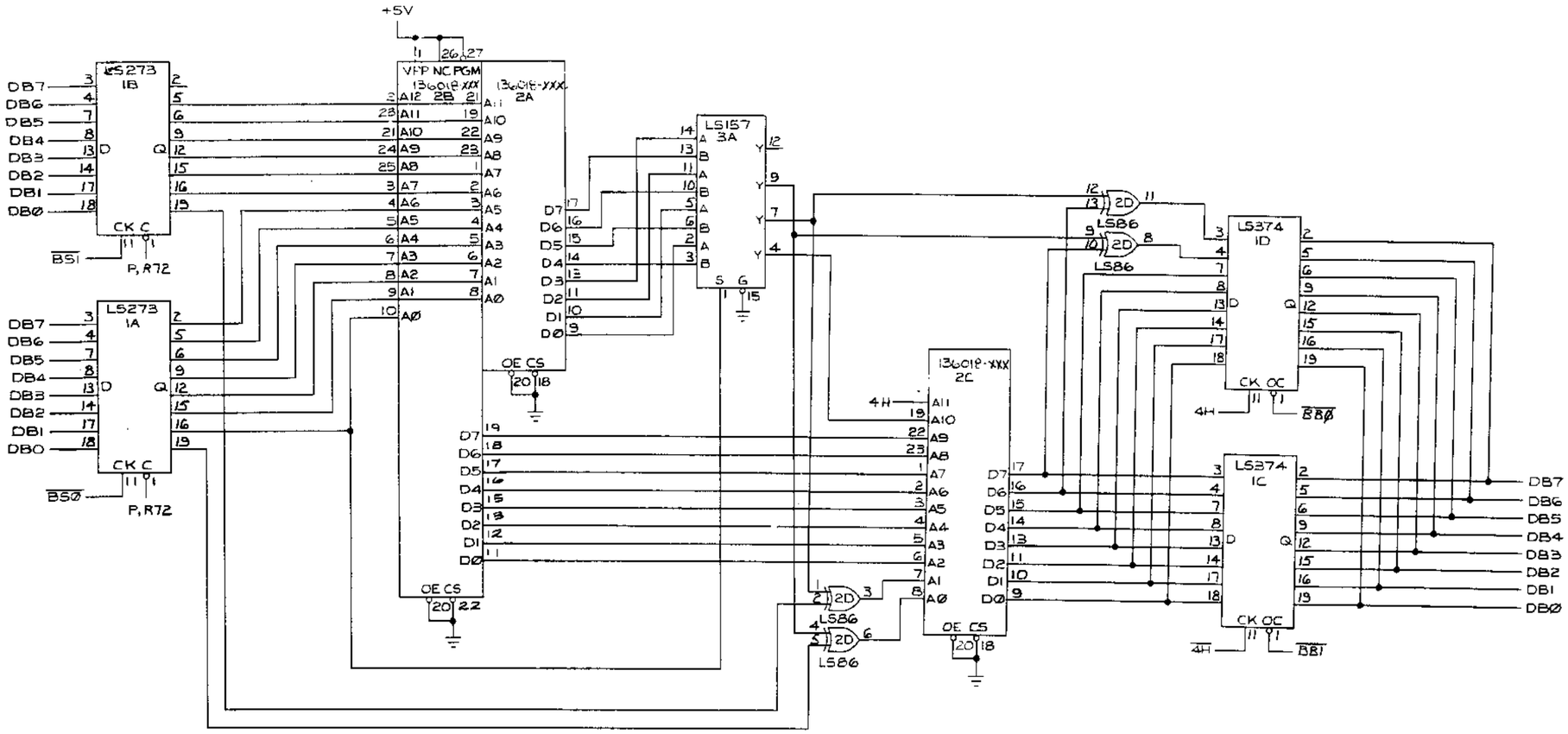
Xevious Video PCB Schematic Diagram

Sheet 8A



Xevious Video PCB Schematic Diagram

Sheet 9A



Xevious Video PCB Schematic Diagram

Sheet 9B